AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended): A semiconductor wafer device comprising:

a semiconductor wafer ~~having~~ comprising a circuit area disposed in a central area of said semiconductor

wafer and a peripheral area of said semiconductor wafer not formed with circuits;

a number of semiconductor elements formed in [[the]] said circuit area;

a circuit multi-layer wiring structure formed in [[the]] said circuit area and ~~having~~ comprising multi-layer wirings connected to said semiconductor elements and interlevel insulating films, at least some of [[the]] said multi-layer wirings being damascene wirings including wiring patterns and via conductors embedded in [[the]] said interlevel insulating films; and

a peripheral multi-layer structure formed in [[the]] said peripheral area, ~~having~~ comprising insulating films made of a same materials as [[the]] said interlevel insulating films and one or more conductor filled trenches forming conductor patterns, defined between sidewalls of said insulating films, made of same materials as [[the]] said wiring patterns and not having conductor patterns corresponding to [[the]] said via conductors.

Claim 2 (withdrawn): The semiconductor wafer device according to claim 1, wherein at least one of the interlevel insulating films and at least one of the insulating films corresponding to at least one layer of the multi-layer wirings each includes a first etching stopper layer, a first insulating layer, a second insulating layer and a third insulating layer, the wiring patterns and the conductor patterns are disposed in grooves formed through the third and second insulating layers, and the via conductors are disposed in holes formed through the first insulating layer and the first etching stopper layer.

Claim 3 (withdrawn): The semiconductor wafer device according to claim 2, wherein the second insulating layer is a second etching stopper layer and the first and third insulating layers are silicon oxide layers.

Claim 4 (withdrawn): The semiconductor wafer device according to claim 2, wherein the second insulating layer is an insulating layer having a dielectric constant lower than silicon oxide, and the third insulating layer is an insulating layer having a dielectric constant higher than the second insulating layer.

Claim 5 (withdrawn): The semiconductor wafer device according to claim 2, wherein each of the wiring patterns and via conductors formed in the circuit area is made of a barrier metal layer

covering a continuous inner surface of each of the grooves and holes and an oxidizable metal layer filled in each of the grooves and holes.

Claim 6 (withdrawn): The semiconductor wafer device according to claim 2, wherein each of the via conductors formed in the circuit area is made of a barrier metal layer covering a continuous inner surface of each of the holes, and each of the wiring patterns is made of a barrier metal layer covering a continuous inner surface of each of the grooves and an oxidizable metal layer filled in each of the grooves.

Claim 7 (withdrawn): The semiconductor wafer device according to claim 4, wherein the second insulating layer is removed in the peripheral area and the third insulating layer is formed covering an outermost side wall of the second insulating layer.

Claim 8 (withdrawn): The semiconductor wafer device according to claim 4, wherein the second insulating layer is removed in the peripheral area and a conductive layer same as the wiring pattern and conductor pattern is formed covering an outermost side wall of the second insulating layer.

Claim 9 (withdrawn): The semiconductor wafer device according to claim 2, wherein said multi-layer wiring structure has lower level wiring patterns formed under the first etching stopper layer and made of oxidizable metal.

Claim 10 (withdrawn): A method of manufacturing a semiconductor wafer device, comprising the steps of:

(a) forming lower wiring patterns over a semiconductor wafer having semiconductor elements formed in a circuit area, the lower wiring patterns being connected to the semiconductor elements;

(b) forming an interlevel insulating film over the semiconductor wafer, the interlevel insulating film covering the lower wiring patterns and having a planarized surface; and

(c) forming via conductors connected to the lower wiring patterns, wiring patterns disposed on the via conductors in the circuit area and conductor patterns made of a same material as the wiring patterns in a peripheral area other than the circuit area, by embedding the via conductors, wiring patterns and conductor patterns in the interlevel insulating film, the conductive patterns being electrically isolated.

Claim 11 (withdrawn): The method of manufacturing a semiconductor wafer device according to claim 10, wherein:

said step (b) includes a step of sequentially laminating a first etching stopper layer, a first insulating layer having a planarized surface, a second insulating layer and a third insulating layer; and

said step (c) includes a step (c-1) of selectively removing the third and second insulating layers to form wiring pattern grooves in the circuit area and conductor pattern grooves in a peripheral area other than the circuit area, a step (c-2) of forming holes through the first insulating layer and the first etching stopper layer in the circuit area, each hole extending from a bottom of the wiring pattern groove to the lower wiring pattern, and a step (c-3) of filling conductors in the wiring pattern grooves, holes and conductor pattern grooves.

Claim 12 (withdrawn): The method of manufacturing a semiconductor wafer device according to claim 10, wherein:

said step (b) includes a step (b-1) of laminating a first etching stopper layer and a first insulating layer, a step (b-2) of polishing the first insulating layer to planarize an upper surface of the first insulating layer, and a step (b-3) of laminating a second insulating layer and a third insulting layer on the planarized surface; and

said step (c) includes a step (c-1) of forming holes through the first insulating layer and first etching stopper layer in the circuit area to expose surfaces of the lower wiring patterns, after said step (b-2), a step (c-2) of filling via conductors in the holes, a step (c-3) of selectively removing the third and second insulating layers to form wiring pattern grooves exposing surfaces of the via conductors

in the circuit area and conductor pattern grooves in a peripheral area other than the circuit area, after said step (b-3), and a step (c4) of filling conductors in the wiring pattern grooves and conductor pattern grooves.

Claim 13 (withdrawn): The method of manufacturing a semiconductor wafer device according to claim 11, wherein:

said step (b) includes a step (b-1) of laminating an etching stopper layer and a first insulating layer, a step (b-2) of planarizing an upper surface of the first insulating layer, and a step (b-3) of laminating a second insulating layer having a lower dielectric constant than silicon oxide on the planarized first insulating layer and a third insulating layer having a dielectric constant higher than the lower dielectric constant; and

said step (c) includes a step of covering an outermost side wall of the second insulating layer with the third insulating layer or the conductor.

Claim 14 (withdrawn): The method of manufacturing a semiconductor wafer device according to claim 11, wherein:

said step (b) includes a step (b-1) of forming a first insulating layer having a lower dielectric constant lower than silicon oxide, a step (b-2) of removing the first insulating layer in the peripheral area, and a step (b-3) of forming a second insulating layer having a dielectric constant higher than the lower dielectric constant on the semiconductor wafer; and

said step (c) includes a step of covering an outermost side wall of the first insulating layer with the second insulating layer or the conductor.

Claim 15 (withdrawn): A method of manufacturing a semiconductor wafer device, comprising the steps of:

(a) forming a first insulating layer having a lower dielectric constant than silicon oxide over an underlying structure including a semiconductor wafer;

(b) removing the first insulating layer in a peripheral area of the semiconductor wafer;

(c) forming a second insulating layer having a higher dielectric constant than the first insulating layer, the second insulating layer covering an outermost side wall of the first insulating layer;

(d) forming wiring grooves at least through the second insulating layer;

(e) forming a conductive layer on the second insulating layer; and

(f) polishing the conductive layer to leave wiring patterns in the wiring grooves and to form a configuration wherein an outermost side wall of the first insulating layer is covered with the second insulating layer or the conductive layer.

Claim 16 (withdrawn): The method of manufacturing a semiconductor wafer device according to claim 15, wherein said step (d) leaves the second insulating layer covering the

outermost side wall of the first insulating layer, and said step (f) covers the outermost side wall of the first insulating layer with the second insulating layer.

Claim 17 (withdrawn): The method of manufacturing a semiconductor wafer device according to claim 15, wherein said step (d) exposes the outermost side wall of the first insulating layer outside the wiring grooves, said step (e) forms the conductive layer which is thicker in a peripheral area than in a central area of the semiconductor wafer, and said step (f) leaves the conductive layer covering the outermost side wall of the first insulating layer.

Claim 18 (withdrawn): The method of manufacturing a semiconductor wafer device according to claim 15, further comprising the steps of:

(g) forming an etching stopper layer and a lower insulating layer before said step (a); and

(h) forming via holes continuous with the wiring grooves through the lower insulating layer and the etching stopper layer.

Claim 19 (withdrawn): The method of manufacturing a semiconductor wafer device according to claim 18, further comprising a step of:

(h) planarizing the lower insulating layer after said step (g), wherein said steps (e) and (f) form damascene wirings.

Claim 20 (withdrawn): The method of manufacturing a semiconductor wafer device according to claim 15, wherein the first insulating layer having the lower dielectric constant is one of a coating type insulating layer, a silicon oxide film containing fluorine or carbon, and a porous insulating layer.

Claim 21 (currently amended): A semiconductor wafer device, comprising:

an underlying structure including a semiconductor wafer;

a first insulating layer having a lower dielectric constant than silicon oxide and formed over said underlying structure in an area excepting a peripheral area of said underlying structure;

a second insulating layer having a dielectric constant higher than said first insulating layer and formed on said first insulating layer;

wiring grooves formed at least through said second insulating layer;

patterns of conductor filled in said wiring grooves; [[and]]

said second insulating layer or a layer of a same material as the conductor covering an outermost side wall of said first insulating layer, and wherein

a multi-layer peripheral structure is formed is said peripheral area not formed with circuits, comprising one or more conductor filled trenches forming conductor patterns.

Claim 22 (currently amended): The semiconductor wafer device according to claim 1, wherein:

said interlevel insulating films include a first insulating layer having a lower dielectric constant than silicon oxide and formed over said semiconductor wafer in an area ~~excepting a~~ except said peripheral area ~~of said underlying structure~~, and a second insulating layer having a dielectric constant higher than said first insulating layer and formed on said first insulating layer and [[the]] said device further comprises said second insulating layer or a layer of a same material as the conductor covering an outermost side wall of said first insulating layer.